911210 1 號

（請續）專利証附件

年 審

中華民國專利公報 (19)(12)

(44)中華民國80年(1991)01月21日

發明

全 7 頁

(51)Int·Cl·：G09G·H01J

(54)名　　稱：在一液晶顯示器上顯示不同灰色深淺度之方法與裝置

(21)申請案號：78107405　　(22)申請日期：中華民國78年(1989)09月26日

(72)發明人：湯姆士H・卡瑞特　　美國

(71)申請人：康培克電腦公司　　美國

(74)代理人：林鐵群　先生

[57]申請專利範圍：

1.一種用以在一顯示裝置上產生一視覺灰度影像之顯示控制系統，該顯示裝置具有一顯示元素陣列，每一元素能響應於一第一或第二種信號位階而分別呈現第一或第二種視覺狀態，該顯示元素陣列具有多數列與多數行，該系統包含：

用以產生該等顯示元素產生一特定顏色之灰度影像之個別顯示信號的裝置，該等顯示信號包含：每一信號具有一各別相對應於該第一或第二信號位階之位元態樣的各數位信號、一預定之態樣週期以及一有關於在該各別顯示元素之位置上之該影像的視覺灰度的工作週期；每一該等數位信號之各位元態樣被重複產生，該用以產生各顯示信號之裝置將該等顯示信號之各連續位元提供給在各連續時框中之各別顯元素；在每一時框中，每一該等顯示信號之其中一位元依序地從該列之一第一個至一最後一個顯示元素提供給在每一列中連貫之各顯示元素，並提供給該陣列中之自一第一列至一最後一列之各連貫列；該裝置並在每次一各別之顯示信號之一位元被提供給一列之該最後一個顯示元素時造成每一後續產生之具有一可與一列中之顯示元素總數整除之態樣週期的顯示信號一預定偏移；該裝置並在每次一各別之顯示信號之一位元提供給該陣列之該最後一列之該最後一個顯示元素時造成每一後續產生之具有一可與該陣列中之顯示元素總數整除之態樣週期的顯示信號一預定偏移。

2.如申請專利範圍第1項所述之顯示控制系統，其中該顯示裝置為一液晶顯示(LCD)板，且該顯示元素陣列包含該LCD板之各播描點陣列。

3.如申請專利範圍第1項所述之顯示控制系統，其中該用以產生該等顯示元素之該等顯示信號的裝置包括：

用以同時產生多數個串列數位信號之裝置，其中每一信號具有一各別相對應於該第一或該第二個信號位階之多個位元態樣、一預定態樣週期以及一不同之工作週期；

用以產生該第一與該第二種信號位階之裝置；

一裝置，用以在每一時框中將位址資料提供給該陣列之各連貫列中之各連續定位且連貫之各顯示元素，而其提供係自該第一列之第一個顯示元素開始至該最後一列之該最後一個顯示元素，並提供與每一被定址之顯示元素有關之顏色屬性資料、一在用以將一列之該最後一個顯示元素定址之位址資料被提供時之列結束信號、以

及一在用以將該最後一列之該最後一個顯示元素定址之位址資料被提供時之框結束信號；以及

顯示信號選擇裝置，其響應於該位址資料以及該用以選擇該第一或第二種信號位階之顏色屬性資料，或是該等多數個具有一關於在該顯示元素被定址之位置處之影像視覺灰度的工作週期的串列數位信號之其中一個的一各別位元；且其中該用以產生該等多數個串列數位信號之裝置係響應於該列結束信號，用以將每一後續產生之具有一可與一列之顯示元素數整除之態樣週期的數位信號偏移一預定數量之位元位置；該裝置還響應於該框結束信號，用以將每一後續產生之具有一可與該陣列之顯示元素總數整除之態樣週期的數位信號偏移一預定數量之位元位置。

4.如申請專利範圍第3項所述之顯示控制系統，其中該用以產生多數個串列數位信號之裝置包括各別之回饋轉移暫存器裝置，用以產生每一對具有該相同態樣週期與互補位元態樣之串列數位信號。

5.如申請專利範圍第1項所述之顯示控制系統，其中該產生在該顯示裝置上之視覺灰度影像係由一陣列之像素所組成，每一像素由該等顯示元素之一各別一個組成，該影像具有八個灰度位階，該等顯示信號之每一個各具有一3或5之態樣週期與一1／3或2／3、或1／5、2／5、3／5或4／5之工作週，或者一0或1之工作週期，而在此之為0之工作週期係相對應於該第一種視覺狀能，而該為1之工作週期則相對應於該第二種視覺狀態。

6.如申請專利範圍第1項所述之顯示控制系統，其中該產生於該顯示裝置上之視覺灰度影像係由一陣列之像素所組成，每一像素由在各連貫列與各連貫行中之一分離之顯示元素羣所組成，且對於該等像素之每一個而言，一各別之視覺灰度位階係藉由提供該像素之各別顯示信號而交錯地刻畫該像素之該等顯示元素而獲得。

7.如申請專利範圍第6項所述之顯示控制系統，其中該產生於該顯示裝置上之視覺灰

度影像之每一像素係由四羣各別彼此相鄰的顯示元素所組成，每一羣包括兩對對角相鄰之顯示元素，該影像具有六種灰度位階，每一個該等顯示信號分別具有一3或5之態樣週期與一1／3或2／3、或1／5、2／5、3／5或4／5之工作週期，或是一0或1之工作週期；該顯示控制系統產生一對各別之具對於一像素之每一對對角相鄰的顯示元素而言有為相同週期之顯示信號，具該等各別對之顯示信號之工作週期對於每一像素之該兩對對角相鄰的顯示元素而言係為0－0、0－1／5、1／5－1／5、1／5－1／3、1／3－1／3、1／3－2／5、2／5－2／5、1／3－2／3、2／…－2／3、3／5－3／5、3／5－2／3、2／3－2／3、2／3－4／5、4／5－4／5、1－4／5或1－1，其中該為0之工作週期係相對應於該第一種視覺狀態，而該為1之工作週期則相對應於該第二種視覺狀態。

8.一種用以驅動一具有多數個顯示元素之顯示裝置的方法，其每一顯示元素分別響應於一第一或一第二種信號位階而提供一第一或一第二種視覺狀態，此方法係用以產生一視覺灰度影像，而該等顯示元素係放置在具有多數列與多數行的一陣列中，該方法包含以下步驟：

產生該等用以產生一特定顏色之一灰度影像的顯示元素所須之各別顯示信號，該顯示信號包含每一個具有一各別相對於該第一或該第二種信號位階之位元態樣，且具有一預定態樣週期以及一有關於該各別之顯示元素所在位置處之該影像該視覺灰度之工作週期的數位信號，每一該等數位信號之位元態樣被重複產生；

將該等顯示信號之各連續位元在各連續時框中提供給該等顯示元素，在每一框中，每一該等顯示信號之其中一位元依序地從該列之一第一個至一最後一個顯示元素地提供給在每一列中之各連貫顯示元素，並從該陣列之一第一列開始且結束於其最後一列地提供給各連貫列；

5

在每次一各別之顯示信號之位元被提供給該一列之該最後一顯示元素時，使每一後續產生之具有一與一列中之顯示元素總數可以整除之態樣週期的顯示信號造成一預定之偏移；以及

在每次一各別之顯示信號之位元被提供給該陣列之該最後一列之該最後一顯示元素時，使每一後續產生之具有一與該陣列中之顯示元素總數可以整除之態樣週期的顯示信號造成一預定之偏移；藉此，在各連續之時框中，在該陣列之每一列中相鄰之各顯示元素即具有不同順序之第一與第二種信號位階，且在該陣列之每一行中之相鄰顯示元素即具有不同順序之該第一與該第二種信號位階。

9. 如申請專利範圍第8項所述之該用以驅動一顯示裝置之方法，其中該顯示裝置爲一液晶顯示（LCD）板，且該等多數顯示元素爲該 LCD 板之多數掃描點。

10. 如申請專利範圍第8項所述之該用以驅動一顯示裝置之方法，其中該產生各別之顯示信號的步驟包含：產生該第一與該第二種信號位階之步驟，同時產生多數個串列之每一信號具有一各別相對應於該第一或該第二種信號位階之位元態樣的數位信號、一預定之態樣週期、以及一不同之工作週期；且該在各連續時框中將該等顯示信號之各連續位元提供給該等顯示元素之步驟包括以下之步驟：產生用以在每一時框中將在該陣列之各連貫列中之各連貫顯示元素從該第一列之該第一個顯示元素至該最後一列之該最後一顯示元素地連續定址所須之位址資料，產生與每一要被定址之顯示元素相關之顏色屬性資料，在用以將一列之該最後一顯示元素定址之位址資料被產生時產生一列結束信號，在用以將該最後一列之該最後一顯示元素定址之位址資料被產生時產生一框結束信號，並選擇該第一或該第二種信號位階，或是該等多串數列數位信號中具有一代表該在該要被定址之顯示元素之位置處之影像視覺灰度的工作週期之一個的各別位元；且其中每一後續產生之具有一與一列之該顯示元素數可以整除之態樣週期的數位信號將在每次該列結束信號被產生時偏移一預定數量之位元位置，且每一後續產生之具有一與該陣列之顯示元素總數可以整除之態樣週期的數位信號將在每次該框結束信號被產生時偏移一預定數量之位元位置。

6

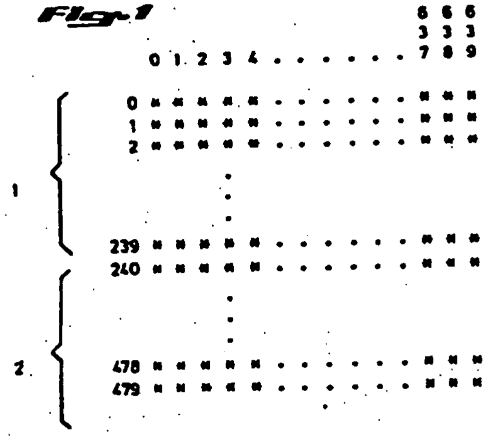
11. 如申請專利範圍第8項所述之該用以驅動一顯示裝置之方法，其中該產生於該顯示裝置上之視覺灰度影像係由一陣列之像素所構成，且每一像素由該等顯示元素之一各別一個組成，該影像具有八個灰度位階，該等顯示信號之每一個各具有一3或5之態樣週期與一1／3或2／3、或1／5、2／5、3／5或4／5之工作週期，或者一0或1之工作週期，而在此之爲0之工作週期係相對應於該第一種視覺狀態，而該爲1之工作週期則相對應於該第二種視覺狀態。

12. 如申請專利範圍第8項所述之該用以驅動一顯示裝置之方法，其中該產生於該顯示裝置上之視覺灰度影像係由一陣列之像素所組成，每一像素由在各連貫列與各連貫行中之一分離之顯示元素所組成，且對於該等像素之每一個而言，一各別之視覺灰度位階係藉由提供該像素之各別顯示信號而交錯地刺激該像素之該等顯示元素而獲得。

13. 如申請專利範圍第12項所述之該用以驅動一顯示裝置之方法，其中該產生於該顯示裝置上視覺灰度影像之每一像素係由四群各別彼此相鄰的顯示元素所組成，每一群包括兩對對角相鄰之顯示元素，該影像具有六種灰度位階，每一個該等顯示信號分別具有一3或5之態樣週期與一1／3或2／3、或1／5、2／5、3／5或4／5之工作週期，或是一0或1之工作週期；該顯示控制系統產生一對各別之具對於一像素之每一對對角相鄰的顯示元素而言有爲相同週期之顯示信號，且該等各

別對之顯示信號之工作週期對於每一像素之該兩對對角相鄰的顯示元素而言係爲0－0、0－1／5、1／5－1／5、1／5－1／3、1／3－1／3、1／3－2／5、2／5－2／5、1／3－2／3、2／5－2／3、3／5－3／5、3／5－2／3、2／3－2／3、2／3－4／5、4／5－4／5、1－4／5或1－1，其中該爲0之工作週期係相對應於該第一種視覺狀態，而該爲1之工作週期則相對應於該第二種視覺狀態。

Fig.1



	0	1	2	3	4	5	6	7	. . .	639
0	1	1	0	1	1	.	.	.	. . .	
1	1	1	0	1	1	.	.	.	. . .	

Fig.2

	0	1	2	3	4	. . .	639
0	1	1	0	1	1	. . .	

Fig.3

	0	1	2	3	4	. . .	639
0	1	1	0	1	1	. . .	

Fig.4

1	0	5	0%
2	1	5	20%
3	1	3	33%
4	2	5	40%
5	3	5	60%
6	2	3	67%
7	4	5	80%
8	5	5	100%

0 1 2 3 4 5 . . .

	0 1 2 3 4 5 6 7 8 . . .	636	637	638	639
0	0 0 1 0 0 1 0 0 1	0	0	1	0
1	0 1 0 0 1 0 0 1 0	0	1	0	0
2	1 0 0 1 0 0 1 0 0	1	0	0	1
3	0 0 1 0 0 1 0 0 1				
	. . . .				
	. . . .				
	. . . .				
239	. . . .				

Fig.5

Fig.7

1	G1	G2	G3	G4	G5 . . .	G4
2	G2	G3	G4	G5	G1 . . .	G5
3	G3	G4	G5	G1	G2 . . .	
4	G4	G5	G1	G2	G3 . . .	G2
5	G5	G1	G2	G3	G4 . . .	G3

4/5

G1	G2	G3	G4	G5
11101111	01111011	11011110	11110111	10111101

Fig.6

3/5

G1	G2	G3	G4	G5
10101101	01101011	01011010	11010110	10110101

Fig.8

1	0	1	2	3	4	5	6 . . .
1	G1	G2	G3	G4	G5	. . . .	
2	G5	G1	G2	G3	G4	. . . .	
3	G4	G5	G1	G2	G3	. . . .	

2	0	1	2	3	4 7
1	G3	G4	G5	G6	G7 . . . .
2	G2	G3	G4	G5	G6 . . . .
3	G1	G2	G3	G4	G5 . . . .

FIG.9

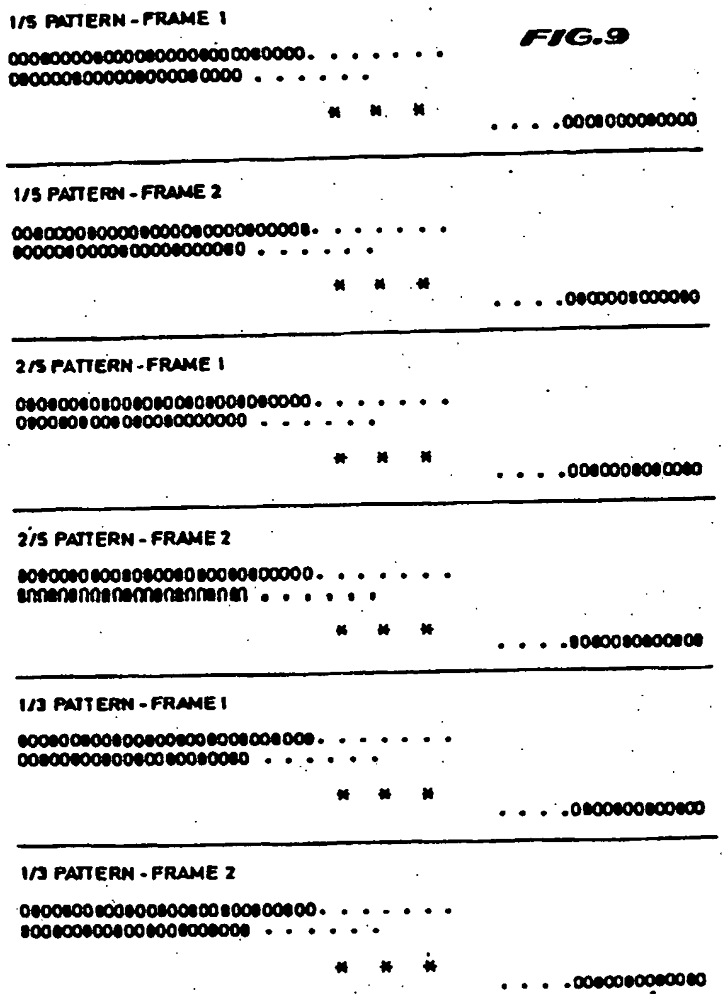


Fig. 10

1.	0	- 0
2.	0	- 1/5
3.	1/5	- 1/5
4.	1/5	- 1/3
5.	1/3	- 1/3
6.	1/3	- 2/5
7.	2/5	- 2/5
8.	1/3	- 2/3
9.	2/5	- 2/3
10.	3/5	- 3/5
11.	3/5	- 2/3
12.	2/3	- 2/3
13.	2/3	- 4/5
14.	4/5	- 4/5
15.	1	- 4/5
16.	1	- 1

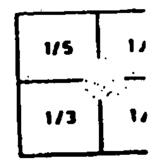
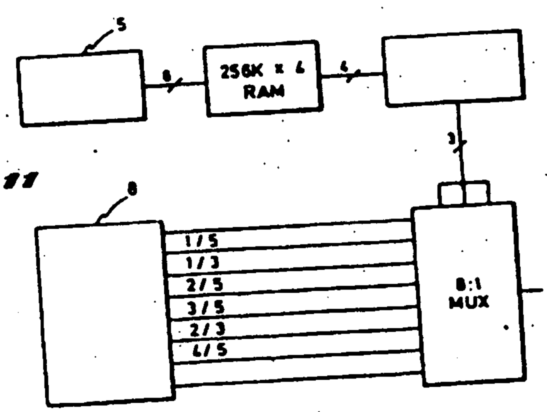


Fig. 11



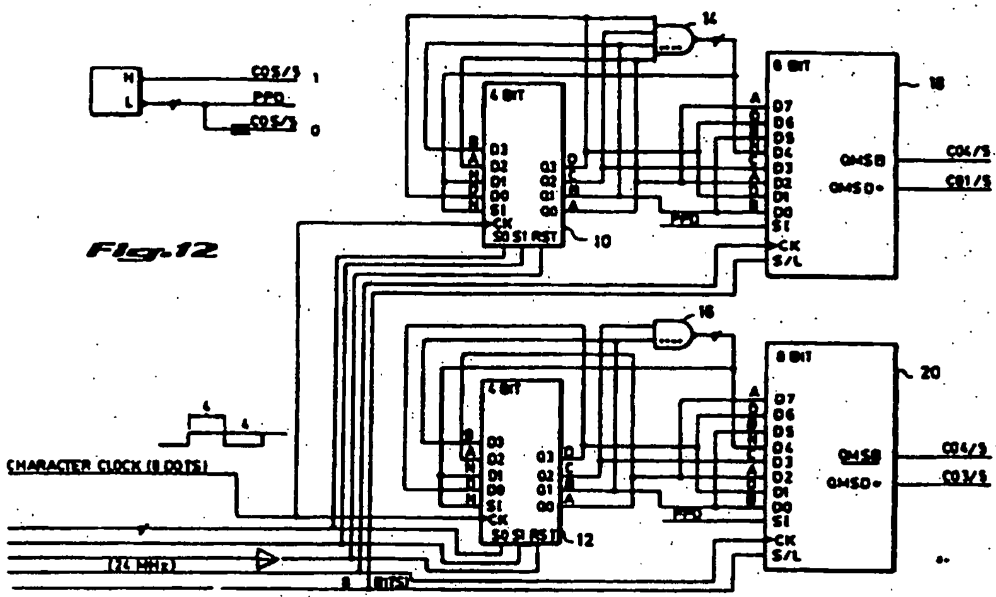


Fig.12

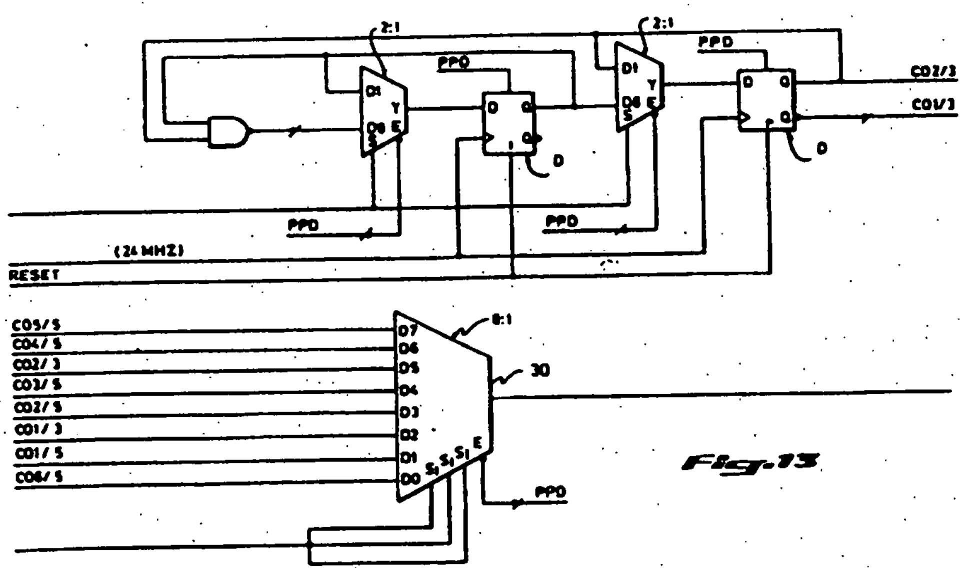


Fig.13

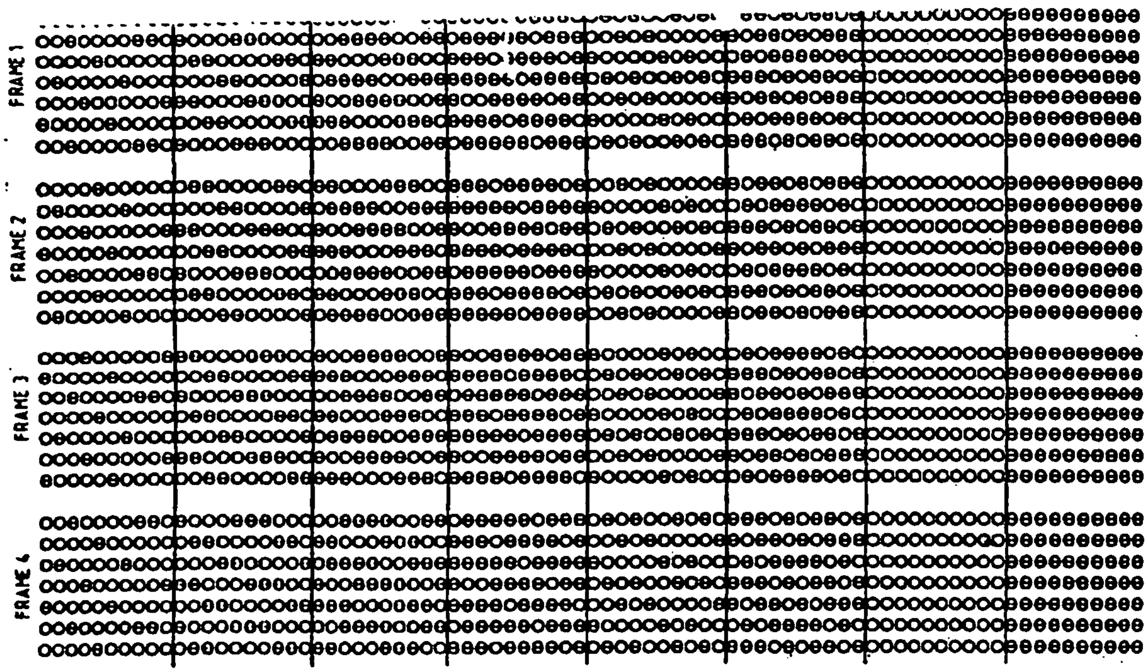


Fig.14

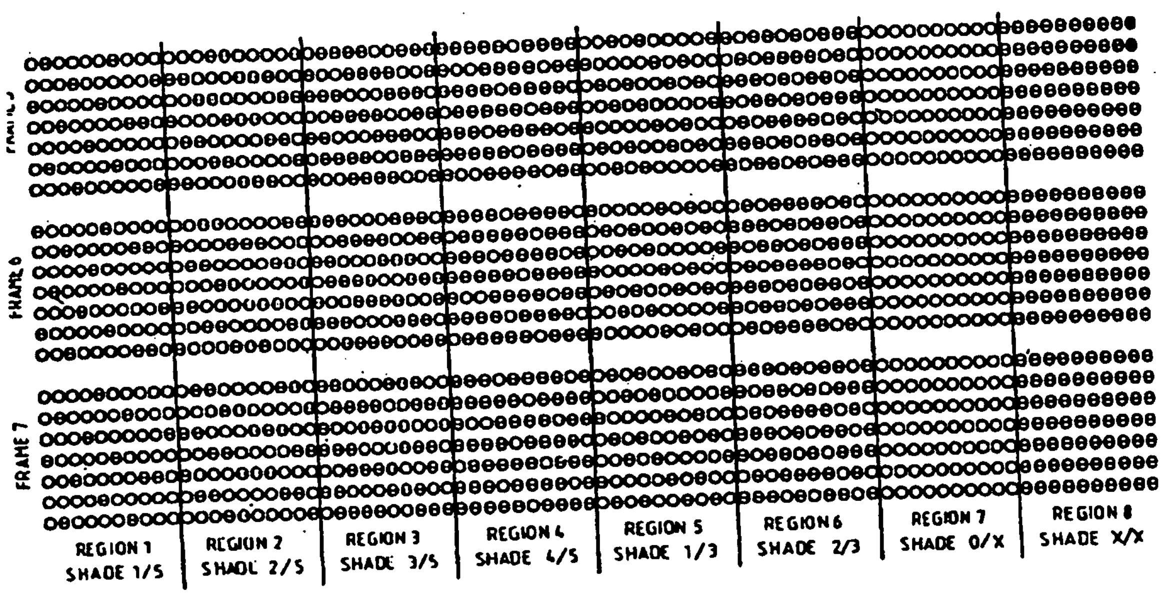


Fig.14A

781074 05

METHOD AND APPARATUS FOR DISPLAYING DIFFERENT SHADES OF GRAY ON A LIQUID CRYSTAL DISPLAY

This invention relates to electronic display panels. More particularly, it relates to display panels comprising liquid crystals and similar display systems having picture elements ("pixels") which normally are selectable in only one of two possible states (e.g., "on" or "off").

Many different types of display panels or screens are used in electronic equipment. One particularly common type is the cathode ray tube (CRT) used in television receivers and many computer monitors. Other available display systems include those which employ incandescent filaments, light-emitting diodes ("LED's"), liquid crystal displays ("LCD's"), plasma display panels, and electroluminescent panels.

CRT's are available in both monochrome and color versions. Inasmuch as many personal computers are equipped with color monitors, much software written for such computers is designed to make use of the color capabilities of the monitor.

When such software is used on a system having only a monochrome monitor, it is customary to "translate" the

colors into various "shades of gray". This term, however, does not necessarily imply that the display is colored gray. Many computer monitors employ green or amber phosphors and hence "shades of gray" actually denotes various intensity levels of those colors.

On a CRT display, various shades of gray (or intensity levels) can be generated simply by varying the intensity of the electron beam impinging on the phosphors of the screen. As this may be accomplished in analog fashion, a virtual continuum of shades of gray is available. Similarly, the intensity of an incandescent filament can be varied by changing the current passing through the filament and drive circuitry is well known which permits the current to be a continuous variable.

In contrast, other display systems employ essentially "two-state" screen dots, i.e., display elements whose intensity at an instant in time cannot normally be continuously varied, but rather are designed to be in one of two possible states e.g., "on" or "off"; "black" or "white", "light" or "dark"; "polarized" or "unpolarized"; etc.

Plainly, such display systems are ideally suited for use with digital computers which operate using the binary number system. A liquid crystal display is an example of such a system.

A problem arises in generating shades of gray on such display systems. Because such systems normally lack intermediate states, "translations" of color displays become difficult or impossible, and at least a portion of the information contained in a display intended for a color monitor is lost.

It might seem that one solution to this problem would simply be to rapidly cycle the various screen dots on and off, varying the on time so as to produce different shades

78107601

of gray. If the cycling were sufficiently rapid, the alternating character would not be perceived by the human eye. In practice, however, there are at least two problems with this approach.

The first problem is that many two-state display systems, particularly LCD's, cannot be rapidly cycled. This may be due to constraints inherent in the drive circuitry and/or the intrinsic time constant of the display. For example, LCDs function by aligning liquid crystal molecules in response to an applied electric field. This alignment takes time to accomplish, and the unalignment of the molecules when the electrical signal is removed or reversed also requires an appreciable time interval.

The second problem arises when the repeat rate (the rate at which the screen display is refreshed) is relatively low, e.g., approximately 70 mHz. The problem is that when an attempt is made to assign different shades of gray to adjacent screen dots using a fixed cycling scheme, a perceptible flicker often results. It is contemplated that this flicker is due to beat frequencies between the two "shades".

The method and apparatus of the present invention provides a means for both spatially and temporally resolving the on/off states of a two-state display device such as an LCD to provide apparent shades of gray. In one embodiment, eight shades of gray are provided. These shades are generated by cycling individual screen dots such that when averaged over time, they are: always off; on 20% of the time; 33% of the time; 40% of the time; 60% of the time; 67% of the time; 80% of the time; or, on at all times.

A feature of the invention is the fact that the cycling between on and off states is not performed in a discernible pattern. For example, the shade of gray corresponding to a screen dot being on 40% of the time can be achieved by selecting the screen dot to be on for 2

cycles out of every five. However, rather than employing a pattern which repeats every five cycles (such as 10010100101001010010100101001010010. . . . .), a pseudo-random pattern is utilized which repeats only after many cycles.

An additional feature of the method of the present invention is that adjacent screen dots, when selected to display the same shade of gray, do not cycle on and off in synchronization, but rather utilize out-of-phase cycling patterns. This spatial resolution reduces perceived flicker in the display and provides a more stable image.

Figure 1 shows a screen dot arrangement of an LCD panel in accordance with the invention. For convenience, the term "pixel" is used synonomously with "screen dot" except where indicated otherwise. The pixels are arranged to form a 640-column by 480-row display, which may be formed from two 640 X 240-pixel subpanels. The terms "row" and "line" are used interchangeably.

Any given pixel is driven to simulate a shade of gray by driving it toward its ON state for a specified length of time, then by driving it toward its OFF state for another specified length of time. For convenience, the basic unit of time is referred to here as a "timeframe," which may be approximately 1/70th of a second.

Flickering and "swimming" (an apparent instability of the picture on a display, somewhat akin to the visual image of a mirage in a desert) may be reduced in accordance with the invention by driving pixels to conform generally to two basic guidelines: (1) no two consecutive lines of pixels should display the same ON-OFF pattern, and (2) any given line of pixels should not display the same ON-OFF pattern in two consecutive timeframes.

In other words, each pixel's on-off display should be modulated both in a temporal dimension and in a spatial dimension.

These guidelines are illustrated in Figures 2 and 3. Assume that a 1 means that the pixel in question is ON and a 0 means the pixel is OFF. The configuration depicted in Figure 2 does not conform to the first guideline. Likewise, the configuration depicted in Figure 3 does not conform to the second guideline.

Two terms are used herein for convenience. A "pattern cycle" is the repetitive period of a given pixel either in the time dimension (expressed in timeframes) or in a spatial dimension (expressed in pixels). A "duty cycle" is the number of timeframes or pixels within a pattern cycle in which the pixel is on, divided by the number of timeframes or pixels in the pattern cycle.

In the time dimension, for example, a pixel that is ON for 3 timeframes and then OFF for 2 timeframes, in a repetitive time pattern, has a pattern cycle of 5 and a duty cycle of 3/5. Pixels in a 3/5 duty cycle are sometimes referred to herein as 3/5 pixels.

Figure 4 depicts a table of specific duty cycles for achieving eight different shades of gray utilizing two pattern cycles, namely 3 and 5, with varying duty cycles.

As noted above, to conform to the guidelines discussed above, each pixel should be modulated at a timeframe rate in both time and space. The pattern cycle of 3 is the simpler of the two cases; the set of all possible duty cycles to achieve this modulation in such a pattern cycle are 0/3, 1/3, 2/3, and 3/3.

In the 0/3 and 3/3 duty cycles, the associated pixels are always off and always on, respectively. Consequently, only the other two duty cycles need be examined.

In the spatial dimension, the other two patterns in the pattern cycle of 3 are the permutations of 001 (which is the 1/3 duty cycle) and the permutations of 110 (which is

the 2/3 duty cycle).

It will be noted that these two patterns are logical inversions of each other. Therefore, only an arbitrary one of them need be discussed; the other can be generated by inverting the other.

The 1/3 duty cycle is discussed here. This duty cycle is implemented as shown in Figure 5. The basic pattern (001) is repeated throughout an entire line.

A possibility that must be taken into account is that a run of pixels in a certain pattern will transcend a row, i.e., that a particular shade of gray, and its associated pixel pattern, will run past the end of one row into another row. This raises the possibility that two consecutive rows might share the same pixel pattern, and thus would not strictly conform to the above guidelines.

This is not a danger for the 1/3 duty cycle: since a line in the illustrative embodiment consists of 640 pixels, and 640 is not an integral multiple of 3, an Nth line of pixels will not have the same pixel pattern as an N+1th line. More particularly, a pixel pattern that begins at pixel 0 of the Nth line will repeat beginning at pixel 639 of that line and will thus be continued at pixels 0 and 1 of the next line. Consequently, the first guideline is automatically satisfied at least as to those two lines.

Note, however, that for any sequence of four or more lines 0 through 3 of the same shade of gray, lines 0 and 3 are identical. This means that each line is repeated at intervals of 3 (i.e., line 0 = line 3, line 1 = line 4, line 2 = line 5, etc.), meaning that a three-line pattern in the same shade of gray would repeat itself. Because 240 (the number of lines on each of the two subpanels in the illustrative embodiment) is an integral multiple of 3, it is possible that the entire screen pattern could be repeated from timeframe to timeframe.

To prevent this, the pixel pattern is skewed or shifted between any two consecutive timeframes. For example, if line 0 begins with 001 in timeframe 1, it begins with 100 in timeframe 2 to avoid a repeating pattern from timeframe to timeframe. This is achieved by setting the pixel (0,0) during timeframe N+1 to be equal to the setting of the pixel (239, 639) during timeframe N. Once this is done, both guidelines are satisfied.

A pattern cycle of 5 is implemented with two basic sequences, a 4/5 sequence and a 3/5 sequence, as shown in Figure 6. It will be noted that the 1/5 and 2/5 sequences are logical inversions of the 4/5 and 3/5 sequences, respectively. Thus, only the latter two will be discussed.

The 640 pixels in a given row are divided into 16 sets of five groups of 8 pixels each (G1 through G5) as a matter of convenience (e.g., to make hardware implementation easier). When the five groups of either sequence are put together, it will be apparent that they do indeed average out to 4/5 on and 3/5 on, respectively.

Since the groups (G1-G5) are each composed of eight bits, a horizontal line of 640 pixels will contain exactly 80 groups. Every line in a 3/5 or 4/5 sequence therefore contains one of the five possible arrangements shown in Figure 7.

Regardless of which arrangement is used, the pattern will repeat line after line and timeframe after timeframe if left alone. This is because 5 divides evenly into both 640 (number of pixels per line) and 240 (number of lines per panel). Skewing prevents repetition of this pattern in a similar manner to that discussed above.

Line-to-line skewing is achieved as follows. If a line I begins with Group N (e.g., G1 is group 1, G2 is group 2, etc.), then the next line I+1 should start with group N-1. If N-1 equals 0, then line I+1 should start with group 5.

Timeframe to timeframe skewing is achieved as follows. If during a timeframe I, a given spatial pixel sequence begins with group N, then during the next timeframe I+1, that pixel sequence should start with group N+2. If N+2 is greater than 5, then during timeframe I+1 the pixel sequence should start with group 1.

An example of how these two rules are utilized is shown in Figure 8. Figure 9 shows a representation of the upper left and lower right hand corners of an LCD display in each of the patterns 1/5, 2/5 and 1/3 between two successive timeframes.

The duty cycles described above advantageously reduce flickering and swimming in other ways. For example, the frequency beating between pixels is reduced. Furthermore, the duty cycles reduce the chance of generating a net DC bias across a pixel (which could damage the pixel).

Conventionally, screen displays are commonly classified as high resolution and low resolution. In high resolution, each pixel is typically composed of one screen dot; in low resolution, each pixel is composed of more than one dot, e.g., a 3X3 dot pattern. The greater number of dots per pixel in low resolution increases the available granularity of gray shading.

In accordance with the invention, using a 2X2 dot pattern as a pixel allows cross-hatching in the conventional manner to produce 16 shades of gray instead of eight. For example, cross-hatching can be used in low resolution to produce a pixel that is darker than a 0 pixel but lighter than a 1/5 pixel. A similar operation can be used to obtain a gray shade between the 1/5 and 1/3 pixels.

Figure 10 sets forth a table of duty cycles that may be used in generating 16 shades of gray. Also shown in Figure 10 is a quartered box representing a 4-dot pixel, each quarter representing a screen dot. In each quarter

of the box, a number is shown that represents the duty cycle for that box for a particular shade of gray, in this case the shade designated by number 4 is Figure 10.

A high-level diagram of apparatus capable of implementing the method of the invention is shown in Figure 11. A video controller 5, not part of the invention, outputs an 8-bit string that specifies which color (out of a possible 256) is desired for display.

A schematic of an illustrative data generator system 8 is depicted in Figures 12 and 13. Two 4-bit shift registers 10 and 12 and corresponding AND gates 14 and 16 operate to generate and rotate the patterns in which screen dots are turned ON and OFF.

The data generator system's normal mode of operation is to rotate the display pattern, with two exceptions. In the case of an end-of-line signal, shown in the Figure as scanline end, the system performs a hold or non-rotate operation, so that the next display pattern generated is the same as the last display pattern generated before the end-of-line signal. In the case of an end-of-screen signal, shown in the Figure as frame end (e.g., a vertical sync signal that in the illustrative embodiment occurs after 240 LCD lines), the data generator system self-loads with the proper bit values so that the pattern will be skewed from timeframe to timeframe.

The 8 bit shift registers 18 and 20 in Figure 12 operate temporarily store the rotated or skewed patterns and send them, one bit at a time, to the 8:1 multiplexer 30 shown in Figure 13. The portion of the data generator system 8 shown in Figure 12 provide all of the shades that have a pattern cycle of 5 (i.e., 0, 1/5, 2/5, 3/5, 4/5, 5/5).

The shades of gray that have a pattern cycle of three (1/3, 2/3) are provided by the circuitry shown in the top half of Figure 13. This configuration simply rotates the

three bit pattern once every cycle. When vertical sync occurs, a hold or non-rotate is performed. The horizontal sync signal need not be considered in this case because line to line skewing is not necessary in the shades that have a pattern cycle of 3.

When all 8 shades (0, 1/5 ... 4/5, 1) are available, they are passed on to the 8:1 multiplexer 30, as shown in Figure 12. The three control lines of the multiplexer then choose one of the eight shades of gray and send it to the LCD panel to be displayed.

Even in low resolution mode, this shading only provides a maximum of 16 different shades. Therefore, the eight bit string will be used to determine which of the 16 cross-hatched shades is desired.

Cross-hatching is actually performed within the low resolution generator. However, if high resolution is desired, then these four bits must pass through the low resolution generator and be further reduced to 3 bits (8 choices). Once this is done, these bits pass on to the multiplexer and one of the eight high resolution shades is chosen and sent to the LCD panel to be displayed.

It will be recognized by those of ordinary skill having the benefit of this disclosure that the embodiments described here are presented for the purpose of illustrating, and not of limiting, the invention defined by the claims set forth below.

For example, Appendix 1 sets forth a computer program written in the BASICA language (Microsoft Corporation, Redmond, Washington) that permits a user to specify one of 8 shades for each of 8 horizontally-disposed regions, thereby to simulate screen output in those shades.

Figure 14 contains a portion of the output of the BASIC simulation program listed in Appendix A. For the particular output listed, 7 timeframes were chosen, each

having an output height of 7 lines. The output may be considered to be a depiction of a portion of an LCD screen (e.g., the first 80 pixels of the first 7 lines in the upper left corner of the pixel array). The 80 pixels shown are divided into 8 regions of 10 pixels each and a different shade is assigned to each region. For the output illustrated in Figure 14, Region 1 is assigned the shade 1/5; region 2 is assigned the shade 2/5; region 3 is assigned the shade 3/5; region 4 is assigned the shade 4/5; region 5 is assigned the shade 1/3; region 6 is assigned the shade 2/3; region 7 is assigned the shade 0/X (i.e., all pixels off at each timeframe); and region 8 is assigned the shade X/X (i.e., all pixels on at each timeframe). Figure 14 depicts a total of 7 timeframes. It will be noted that the pattern repeats every 5 timeframes.

REVISED CLAIMS of R.O.C. Patent No.7810740

Date of Amendment: June, 1990

修正本 79年6月2日 補充

~~1.~~ A display control system for producing an optical gray-scale image on a display device having an array of display elements each providing a first or a second optical state in response to a first or a second signal level, respectively, the array of display elements having a plurality of rows and a plurality of columns, the system comprising:

means for generating respective display signals for the display elements for producing a gray-scale image of a specified color, the display signals comprising digital signals each having a pattern of bits respectively corresponding to the first or the second signal level, a predefined pattern cycle and a duty cycle related to the optical gray-scale of the image at the position of the respective display element, the pattern of bits of each one of the digital signals being repetitively generated, the means for generating display signals providing successive bits of the display signals for respective display elements in successive timeframes, in each timeframe one bit of each of the display signals being provided in sequence for consecutive display elements in each row from a first to a last display element of the row and for consecutive rows beginning at a first row and ending at a last row of the array, and causing a predetermined skewing of each subsequently generated display signal having a pattern cycle for which the total number of display elements in a row is

integrally divisible each time a bit of a respective display signal is provided for the last display element of a row, and causing a predetermined skewing of each subsequently generated display signal having a pattern cycle for which the total number of display elements in the array is integrally divisible each time a bit of a respective display signal is provided for the last display element of the last row of the array.

2. The display control system of claim 1, wherein the display device is a liquid crystal display (LCD) panel and the array of display elements comprises an array of screen dots of the LCD panel.

3. The display control system of claim 1, wherein the means for generating the display signals for the display elements includes:

means for concurrently generating a plurality of serial digital signals each having a pattern of bits respectively corresponding to the first or the second signal levels, a predefined pattern cycle and a different duty cycle;

means for generating the first and the second signal levels;

display control means for providing address data for sequentially addressing consecutive display elements in consecutive rows of the array in each timeframe from the

first display element of the first row to the last display element of the last row, color attribute data associated with each display element being addressed, an end-of-row signal when address data for addressing the last display element of a row is provided, and an end-of-frame signal when address data for addressing the last display element of the last row is provided; and

display signal selection means responsive to the address data and the color attribute data for selecting the first or the second signal level, or a respective bit of one of the plurality of serial digital signals having a duty cycle related to the optical gray-scale of the image at the position of the display element being addressed, and wherein the means for generating the plurality of serial digital signals is responsive to the end-of-row signal for skewing by a predetermined number of bit positions each subsequently generated digital signal having a pattern cycle for which the number of display elements of a row is integrally divisible, and is further responsive to the end-of-frame signal for skewing by a predetermined number of bit positions each subsequently generated digital signal having a pattern cycle for which the total number of display elements of the array is integrally divisible.

4 . The display control system of claim 3 , wherein the means for generating a plurality of serial digital

78107405

signals includes respective feedback shift register means for generating each pair of serial digital signals having the same pattern cycle and complementary patterns of bits.

5. The display control system of claim 1, wherein the optical gray-scale image produced on the display device is composed of an array of pixels each consisting of a respective one of the display elements, the image having eight gray-scale levels and each one of the display signals having a pattern cycle of 3 or 5 and a duty cycle of 1/3 or 2/3, or 1/5, 2/5, 3/5 or 4/5, respectively, or a duty cycle of 0 or 1, where the duty cycle of 0 corresponds to the first optical state and the duty cycle of 1 corresponds to the second optical state.

6. The display control system of claim 1, wherein the optical gray-scale image produced on the display device is composed of an array of pixels each consisting of a separate group of display elements in consecutive rows and consecutive columns, and a respective optical gray-scale level is obtained for each one of the pixels by cross-hatching of the display elements of the pixel by providing respective display signals therefor.

7. The display control system of claim 6, wherein each pixel of the optical gray-scale image produced on the display device consists of a respective group of four

mutually adjacent display elements, including two pairs of diagonally adjacent display elements, the image having sixteen gray-scale levels, each one of the display signals having a pattern cycle of 3 or 5 and a duty cycle of 1/3 or 2/3, or 1/5, 2/5, 3/5 or 4/5, respectively, or a duty cycle of 0 or 1, the display control system generating a respective pair of display signals having the same duty cycle for each diagonally adjacent pair of display elements of a pixel, and the duty cycles of the respective pairs of display signals for the two diagonally adjacent pairs of display elements of each pixel being 0-0, 0-1/5, 1/5-1/5, 1/5-1/3, 1/3-1/3, 1/3-2/5, 2/5-2/5, 1/3-2/3, 2/5-2/3, 3/5-3/5, 3/5-2/3, 2/3-2/3, 2/3-4/5, 4/5-4/5, 1-4/5 or 1-1, where the duty cycle of 0 corresponds to the first optical state and the duty cycle of 1 corresponds to the second optical state.

8. A method for driving a display device having a multiplicity of display elements each providing a first or a second optical state in response to a first or a second signal level, respectively, to produce an optical gray-scale image, the display elements being disposed in an array having a plurality of rows and a plurality of columns, the method comprising the steps of:

generating respective display signals for the display elements for producing a gray-scale image of a specified color, the display signals comprising digital

signals each having a pattern of bits respectively corresponding to the first or the second signal level and having a predefined pattern cycle and a duty cycle related to the optical gray-scale of the image at the position of the respective display element, the pattern of bits of each one of the digital signals being repetitively generated;

providing successive bits of the display signals for the display elements in successive timeframes, in each timeframe one bit of each of the display signals being provided in sequence for consecutive display elements in each row from a first to a last display element of the row, and for consecutive rows beginning at a first row and ending at a last row of the array;

causing a predetermined skewing of each subsequently generated display signal having a pattern cycle for which the total number of display elements in a row is integrally divisible each time a bit of a respective display signal is provided for the last display element of a row; and

causing a predetermined skewing of each subsequently generated display signal having a pattern cycle for which the total number of display elements in the array is integrally divisible each time a bit of a respective display signal is provided for the last display element of the last row of the array, whereby in successive timeframes adjacent display elements in each row of the array are

provided with different sequences of the first and the second signal levels, and adjacent display elements in each column of the array are provided with different sequences of the first and the second signal levels.

9. The method for driving a display device of claim 8, wherein the display device is a liquid crystal display (LCD) panel and the multiplicity of display elements is a multiplicity of screen dots of the LCD panel.

10. The method for driving a display device according to claim 8, wherein the step of generating respective display signals includes the steps of generating the first and the second signal levels, and concurrently generating a plurality of serial digital signals each having a pattern of bits respectively corresponding to the first or the second signal levels, a predefined pattern cycle, and a different duty cycle; and the step of providing successive bits of the display signals for the display elements in successive timeframes includes the steps of: generating address data for sequentially addressing consecutive display elements in consecutive rows of the array in each timeframe from the first display element of the first row to the last display element of the last row, generating color attribute data associated with each display element being addressed, generating an end-of-row signal when address data for

addressing the last display element of a row is generated, generating an end-of-frame signal when address data for addressing the last display element of the last row is generated, and selecting the first or the second signal level, or a respective bit of one of the plurality of serial digital signals having a duty cycle representative of the optical gray-scale of the image at the position of the display element being addressed; and wherein each subsequently generated digital signal having a pattern cycle for which the number of display elements of a row is integrally divisible is skewed by a predetermined number of bit positions each time the end-of-row signal is generated, and each subsequently generated digital signal having a pattern cycle for which the total number of display elements of the array is integrally divisible is skewed by a predetermined number of bit positions each time the end-of-frame signal is generated.

11. The method for driving a display device according to claim 8, wherein the optical gray-scale image produced on the display device is composed of an array of pixels each consisting of a respective one of the display elements, the image having eight gray-scale levels and each one of the display signals having a pattern cycle of 3 or 5 and a duty cycle of 1/3 or 2/3, or 1/5, 2/5 or 4/5, respectively, or a duty cycle of 0 or 1, where the duty

cycle of 0 corresponds to the first optical state and the duty cycle of 1 corresponds to the second optical state.

12. The method for driving a display device according to claim 8, wherein the optical gray-scale image produced on the display device is composed of an array of pixels each consisting of a separate group of display elements in consecutive rows and consecutive columns, and a respective gray-scale level is obtained for each one of the pixels by cross-hatching of the display elements of the pixel by providing respective display signals therefor.

13. The method for driving a display device according to claim 12, wherein each pixel of the optical gray-scale image produced on the display device consists of a respective group of four mutually adjacent display elements, including two pairs of diagonally adjacent display elements, the image having sixteen gray-scale levels, each one of the display signals having a pattern cycle of 3 or 5 and a duty cycle of 1/3 or 2/3, or 1/5, 2/5, 3/5 or 4/5, respectively, or a duty cycle of 0 or 1, the display control system generating a respective pair of display signals having the same duty cycle for each diagonally adjacent pair of display elements of a pixel, and the duty cycles of the respective pairs of display signals for the two diagonally adjacent pairs of display elements of each pixel being 0-0, 0-1/5, 1/5-1/5, 1/5-1/3, 1/3-1/3, 1/3-2/5, 2/5-2/5, 1/3-2/3,

2/5-2/3, 3/5-3/5, 3/5-2/3, 2/3-2/3, 2/3-4/5, 4/5-4/5, 1-4/5 or 1-1, where the duty cycle of 0 corresponds to the first optical state and the duty cycle of 1 corresponds to the second optical state.

ABSTRACT OF THE DISCLOSURE

A method and apparatus are disclosed which provide a means for both spatially and temporally resolving the on/off states of a two-state display device such as a liquid crystal display to provide apparent shades of gray. A particular feature of this method is that the cycling between on and off states is not performed in a discernible pattern. Rather, a pseudo-random pattern is utilized which repeats only after many cycles. Additionally, when the method disclosed herein is utilized, adjacent pixels, when selected to display the same shade of gray, do not cycle on and off in synchronization, but rather utilize out-of-phase cycling patterns. This spatial resolution reduces perceived flicker in the display and provides a more stable image. In one embodiment, eight shades of gray are provided. The shades are generated by cycling individual pixels such that when averaged over time, they are: always off; on 20% of the time; 33% of the time; 40% of the time; 60% of the time; 67% of the time; 80% of the time; or, on at all times.

APPENDIX A

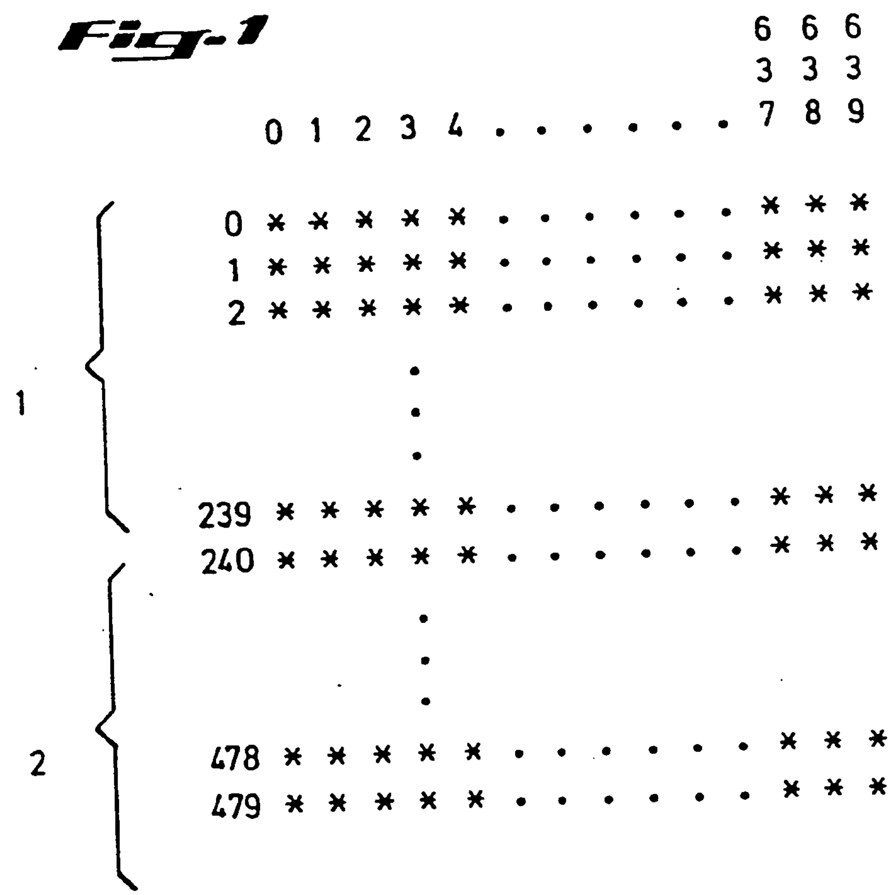
```
1000 PRINT
1010 DIM AVG[80]
1020 GEN5[1,1]=0
1030 GEN5[1,2]=1
1040 GEN5[1,3]=1
1050 GEN5[1,4]=1
1060 GEN5[1,5]=1
1070 GEN5[2,1]=0
1080 GEN5[2,2]=1
1090 GEN5[2,3]=0
1100 GEN5[2,4]=1
1110 GEN5[2,5]=0
1120 GEN3[1]=0
1130 GEN3[2]=1
1140 GEN3[3]=1
1150 FSIZE = 14
1160 OVERWRITE =0
1170 MAXFRAMES = 70
1180 PRINTER =0
1190 FOR X=1 TO 8
1200 CO(X)=X
1210 NEXT X
1220 CLS
1230 INPUT "Do you wish to change display parameters [y] ";A$
1240 IF A$<>"y" AND A$<>"Y" AND A$<>"" THEN GOTO 1440
1250 IF A$="" THEN PRINT "y"
1260 PRINT
1270 INPUT "Enter frame height, no. of frames : ";FSIZE, MAXFRAMES
1280 FSIZE=FSIZE-1
1290 PRINT
1300 INPUT "Should frames be overwritten [y] : ";A$
1310 IF A$="y" OR A$="Y" OR A$="" THEN OVERWRITE =1
1320 IF A$="" THEN PRINT "y"
1330 PRINT
1340 INPUT "Is there a printer to print the results [y] ";A$
1350 IF A$="y" OR A$="Y" OR A$="" THEN PRINTER =1 ELSE PRINTER =0
1360 IF A$="" THEN PRINT "y"
1370 PRINT
1380 PRINT "Please enter gray levels (1-8) to be displayed in regions 1-8"
1390 FOR X=1 TO 8
1400 PRINT "gray level of region ";X;" :";
1410 INPUT CO(X)
1420 NEXT X
1430 REM
1440 REM starting main display loop
1450 REM
1460 SCREEN 1
1470 CLS
```

```
1480 FOR FRAME=1 TO MAXFRAMES
1490 FOR Y=0 TO FSIZE
1500 FOR X=0 TO 79
1510 REM
1520 REM determining pattern that next line should start with and storing it
1530 REM
1540 IF X<>0 THEN 1680
1550 GEN5[1,0]=GEN5[1,5] : GEN5[2,0]=GEN5[2,5]
1560 FOR I=5 TO 1 STEP -1
1570 IF I=1 THEN J=0 ELSE J=I-1
1580 G1[I]=GEN5[1,J]
1590 G2[I]=GEN5[2,J]
1600 NEXT I
1610 IF Y<>0 THEN GOTO 1690
1620 G1[0]=G1[5] : G2[0]=G2[5]
1630 FOR I=5 TO 1 STEP -1
1640 IF I=1 THEN J=0 ELSE J=I-1
1650 FG1[I]=G1[J]
1660 FG2[I]=G2[J]
1670 NEXT I
1680 REM
1690 REM
1700 REM setting 8-bit pattern in PI[] depending upon g-level and gen5[]
1710 REM
1720 GLEVEL = CO[(INT(X/10)+1)]
1730 IF (GLEVEL>4) OR (GLEVEL<1) THEN GOTO 1840
1740 IF (GLEVEL=4) OR (GLEVEL=1) THEN GENNUM = 1 ELSE GENNUM = 2
1750 PI[1]=GEN5[GENNUM,1]
1760 PI[2]=GEN5[GENNUM,4]
1770 PI[3]=GEN5[GENNUM,2]
1780 PI[4]=GEN5[GENNUM,5]
1790 PI[5]=GEN5[GENNUM,3]
1800 PI[6]=GEN5[GENNUM,1]
1810 PI[7]=GEN5[GENNUM,4]
1820 PON=PI[X+1-8*INT(X/8)]
1830 PI[8]=GEN5[GENNUM,2]
1840 CNT=CNT+1
1850 IF CNT<4 THEN GOTO 1950
1860 REM
1870 REM rotating gen3
1880 REM
1890 GEN3[0]=GEN3[1]
1900 FOR I=1 TO 3
1910 IF I=3 THEN J=0 ELSE J=I+1
1920 GEN3[I]=GEN3[J]
1930 NEXT I
1940 CNT=0
```

```
1950 REM
1960 REM setting square of six pixels on or off that simulate 1 pixel on lcd
1970 REM
1980 IF GLEVEL=8 THEN PON=1 ELSE IF GLEVEL=7 THEN PON=0
1990 IF (GLEVEL=5) OR (GLEVEL=6) THEN PON = GEN3[1+X-3*INT(X/3)]
2000 IF GLEVEL=1 OR GLEVEL =3 OR GLEVEL =5 THEN IF PON=1 THEN PON=0 ELSE PON=1
2010 IF Y=0 THEN AVG[X]=PON+AVG[X]
2020 YC=2*(Y+FDISP)
2030 XC=3*X
2040 PSET(XC,YC),PON
2050 PSET(XC+1,YC),PON
2060 PSET(XC+1,YC+1),PON
2070 PSET(XC,YC+1),PON
2080 PSET(XC+2,YC),PON
2090 PSET(XC+2,YC+1),PON
2095 IF PON=1 THEN LPRINT CHR$(233); ELSE LPRINT CHR$(79);
2100 REM
2110 REM rotating gen5 (1 & 2)
2120 REM
2130 CNT8=CNT8+1
2140 IF CNT8<8 THEN GOTO 2220
2150 GEN5[1,0]=GEN5[1,1] : GEN5[2,0]=GEN5[2,1]
2160 FOR I=1 TO 5
2170 IF I=5 THEN J=0 ELSE J=I+1
2180 GEN5[1,I]=GEN5[1,J]
2190 GEN5[2,I]=GEN5[2,J]
2200 NEXT I
2210 CNT8=0
2220 NEXT X
2230 FOR L=1 TO 5
2240 GEN5[1,L]=G1[L]
2250 GEN5[2,L]=G2[L]
2260 NEXT L
2270 NEXT Y
2280 FDISP=FDISP+FSIZE+3
2290 IF OVERWRITE =1 OR (FDISP+FSIZE)>90 THEN FDISP=0
2300 FOR L=1 TO 5
2310 GEN5[1,L]=FG1[L]
2320 GEN5[2,L]=FG2[L]
2330 NEXT L
2335 LPRINT
2340 NEXT FRAME
2350 SCREEN 2
2360 PRINT
2365 LPRINT CHR$(12)
2370 IF PRINTER=1 THEN LPRINT
2380 PRINT "starting pattern of gen5-1 :";
2390 IF PRINTER=1 THEN LPRINT "starting pattern of gen5-1 :";
```

```
2400 FOR X=1 TO 5
2410 PRINT GEN5[1,X];
2420 IF PRINTER=1 THEN LPRINT GEN5[1,X];
2430 NEXT X
2440 PRINT
2450 IF PRINTER=1 THEN LPRINT
2460 PRINT "starting pattern of gen5-2 :";
2470 IF PRINTER=1 THEN LPRINT "starting pattern of gen5-2 :";
2480 FOR X=1 TO 5
2490 PRINT GEN5[2,X];
2500 IF PRINTER=1 THEN LPRINT GEN5[2,X];
2510 NEXT X
2520 PRINT
2530 IF PRINTER=1 THEN LPRINT
2540 PRINT
2550 IF PRINTER=1 THEN LPRINT
2560 PRINT "Following pixel-on time averages over ";MAXFRAMES;"frames"
2570 IF PRINTER=1 THEN LPRINT "Following pixel on time averages over ";MAXFRAMES;"frames"
2580 PRINT
2590 IF PRINTER=1 THEN LPRINT
2600 PRINT "pixel","color","avg. on"
2610 IF PRINTER=1 THEN LPRINT "pixel","color","avg. on"
2620 FOR X=0 TO 79
2630 PRINT X, CO[INT(X/10)+1], AVG[X]/MAXFRAMES
2640 IF PRINTER=1 THEN LPRINT X, CO[INT(X/10)+1], AVG[X]/MAXFRAMES
2650 NEXT X
```

Fig-1


6 6 6
3 3 3
0 1 2 3 4 . . . . 7 8 9
0 * * * * * . . . . . . * * *
1 * * * * * . . . . . . * * *
2 * * * * * . . . . . . * * *
239 * * * * * . . . . . . * * *
240 * * * * * . . . . . . * * *
478 * * * * * . . . . . . * * *
479 * * * * * . . . . . . * * *
1
2

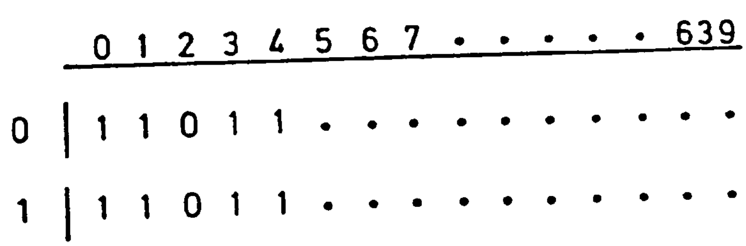

0 1 2 3 4 5 6 7 639
0 1 1 0 1 1 . . . .
1 1 1 0 1 1 . . . .

Fig-2

1:

	0	1	2	3	4	. . . .	639
0	1	1	0	1	1	. . . .	

Fig. 3

	0	1	2	3	4	. . . .	639
0	1	1	0	1	1	. . . .	

Fig. 4

1	0	5	0%
2	1	5	20%
3	1	3	33%
4	2	5	40%
5	3	5	60%
6	2	3	67%
7	4	5	80%
8	5	5	100%

	0	1	2	3	4	5	6	7	8	....	636	637	638	639
0	0	0	1	0	0	1	0	0	1	....	0	0	1	0
1	0	1	0	0	1	0	0	1	0	....	0	1	0	0
2	1	0	0	1	0	0	1	0	0	....	1	0	0	1
3	0	0	1	0	0	1	0	0	1	....				
	....													
	....													
	....													
239	....													

Fig. 5

4/5

G1	G2	G3	G4	G5
11101111	01111011	11011110	11110111	10111101

Fig. 6

3/5

G1	G2	G3	G4	G5
10101101	01101011	01011010	11010110	10110101

	0	1	2	3	4	5 . . . 80	

Fig.7

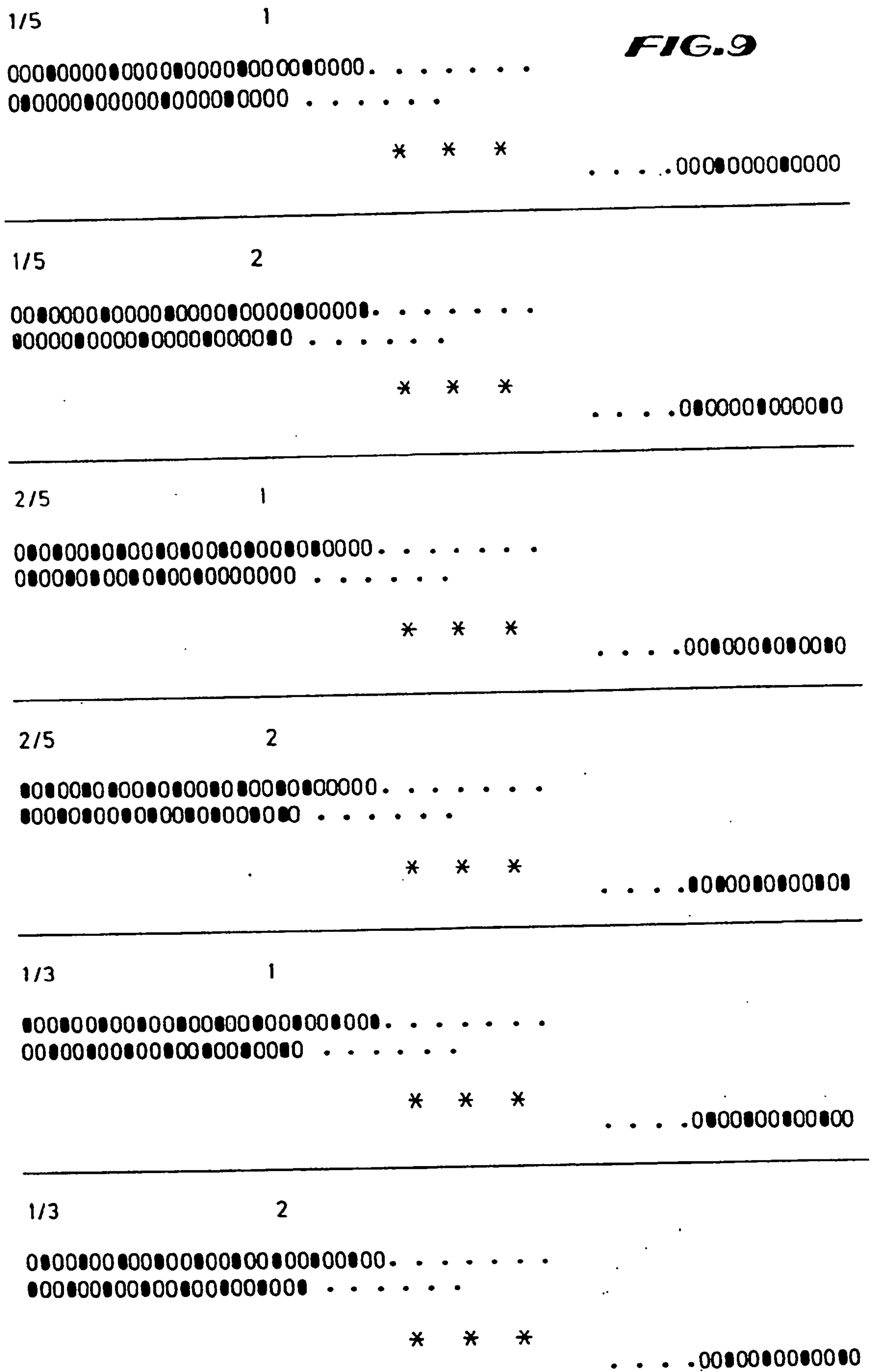
1	G1	G2	G3	G4	G5 . . .	G4	G5
2	G2	G3	G4	G5	G1 . . .	G5	G1
3	G3	G4	G5	G1	G2 . . .	G1	G2
4	G4	G5	G1	G2	G3 . . .	G2	G3
5	G5	G1	G2	G3	G4 . . .	G3	G4

1	0	1	2	3	4	5	6 . . . 79
1	G1	G2	G3	G4	G5		G5
2	G5	G1	G2	G3	G4		G4
3	G4	G5	G1	G2	G3		G3

Fig.8

2	0	1	2	3	4 79
1	G3	G4	G5	G6	G7 . . . . G2
2	G2	G3	G4	G5	G6 . . . .
3	G1	G2	G3	G4	G5 . . . .

FIG.9

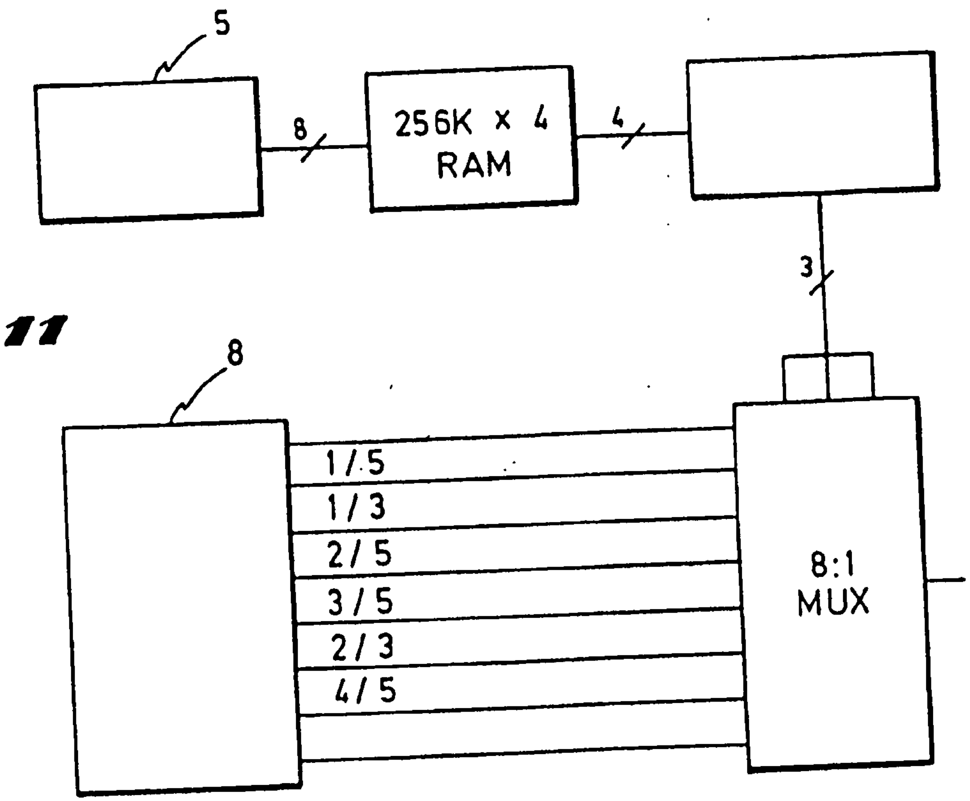


1.	0	-	0
2.	0	-	1/5
3.	1/5	-	1/5
4.	1/5	-	1/3
5.	1/3	-	1/3
6.	1/3	-	2/5
7.	2/5	-	2/5
8.	1/3	-	2/3
9.	2/5	-	2/3
10.	3/5	-	3/5
11.	3/5	-	2/3
12.	2/3	-	2/3
13.	2/3	-	4/5
14.	4/5	-	4/5
15.	1	-	4/5
16.	1	-	1

Fig. 10

1/5	1/3
1/3	1/5

Fig.11



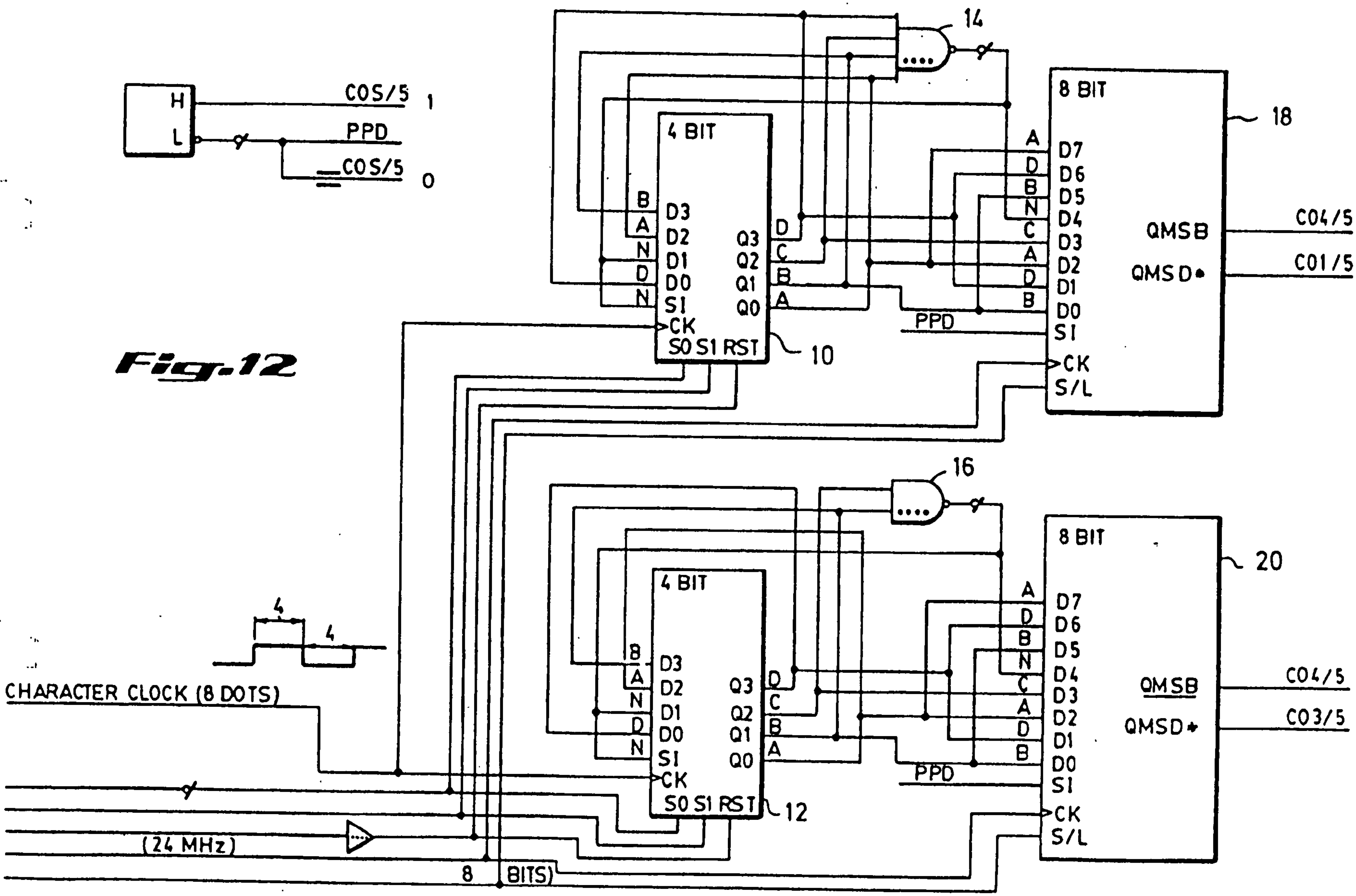

H
L
COS/5
1
PPD
COS/5
0
4 BIT
D3
D2
D1
D0
S1
CK
S0 S1 RST
Q3
Q2
Q1
Q0
10
14
8 BIT
D7
D6
D5
D4
D3
D2
D1
D0
S1
CK
S/L
QMSB
QMSD*
18
C04/5
C01/5
16
12
20
C03/5
CHARACTER CLOCK (8 DOTS)
(24 MHz)
8
BITS)

Fig-12

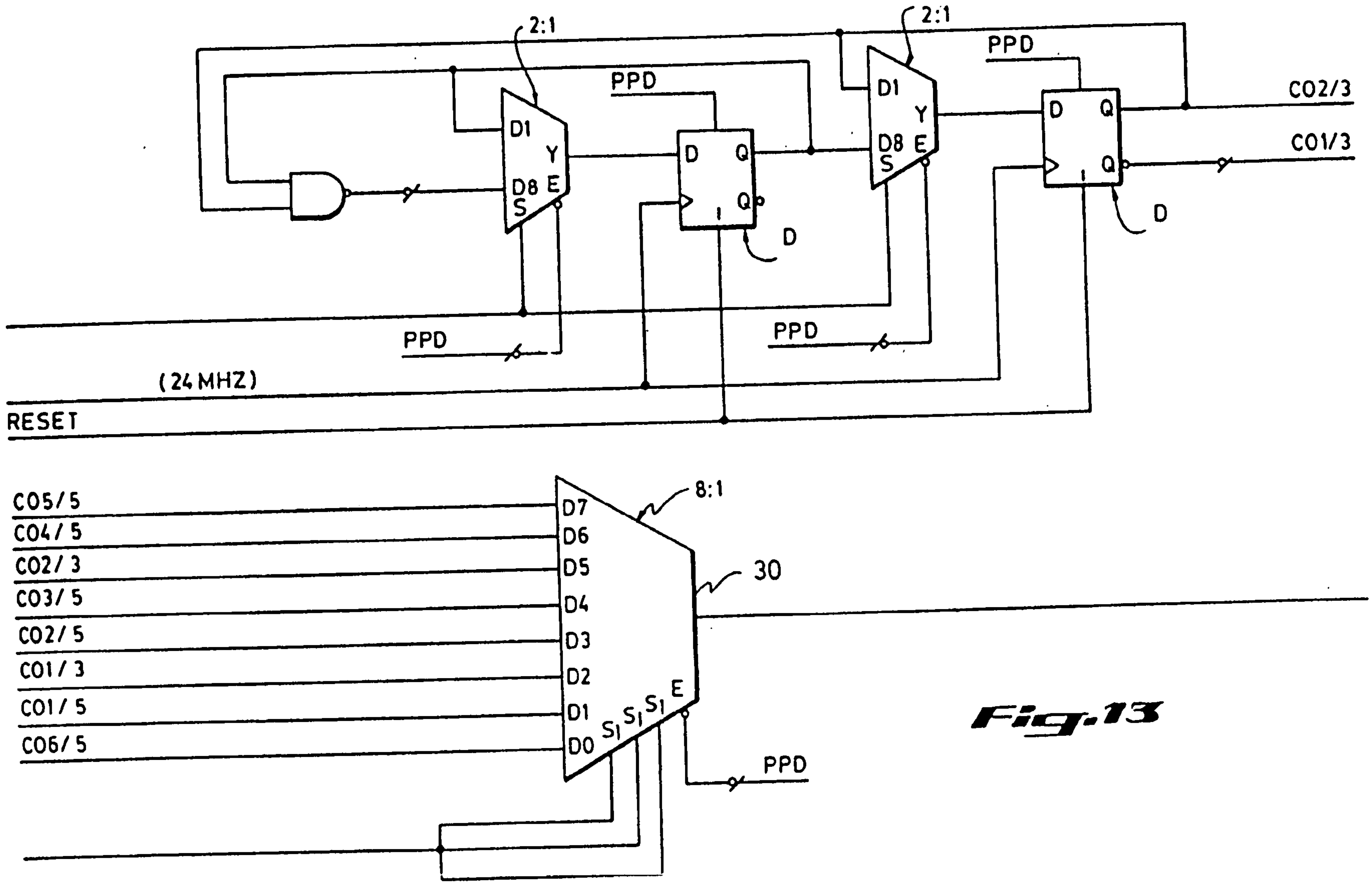

2:1
2:1
PPD
PPD
D1
Y
D8
S
E
D
Q
Q
D
CO2/3
CO1/3
D
D
PPD
PPD
(24 MHZ)
RESET
8:1
30
CO5/5
CO4/5
CO2/3
CO3/5
CO2/5
CO1/3
CO1/5
CO6/5
D7
D6
D5
D4
D3
D2
D1
D0
S1
S1
S1
E
PPD

Fig.13

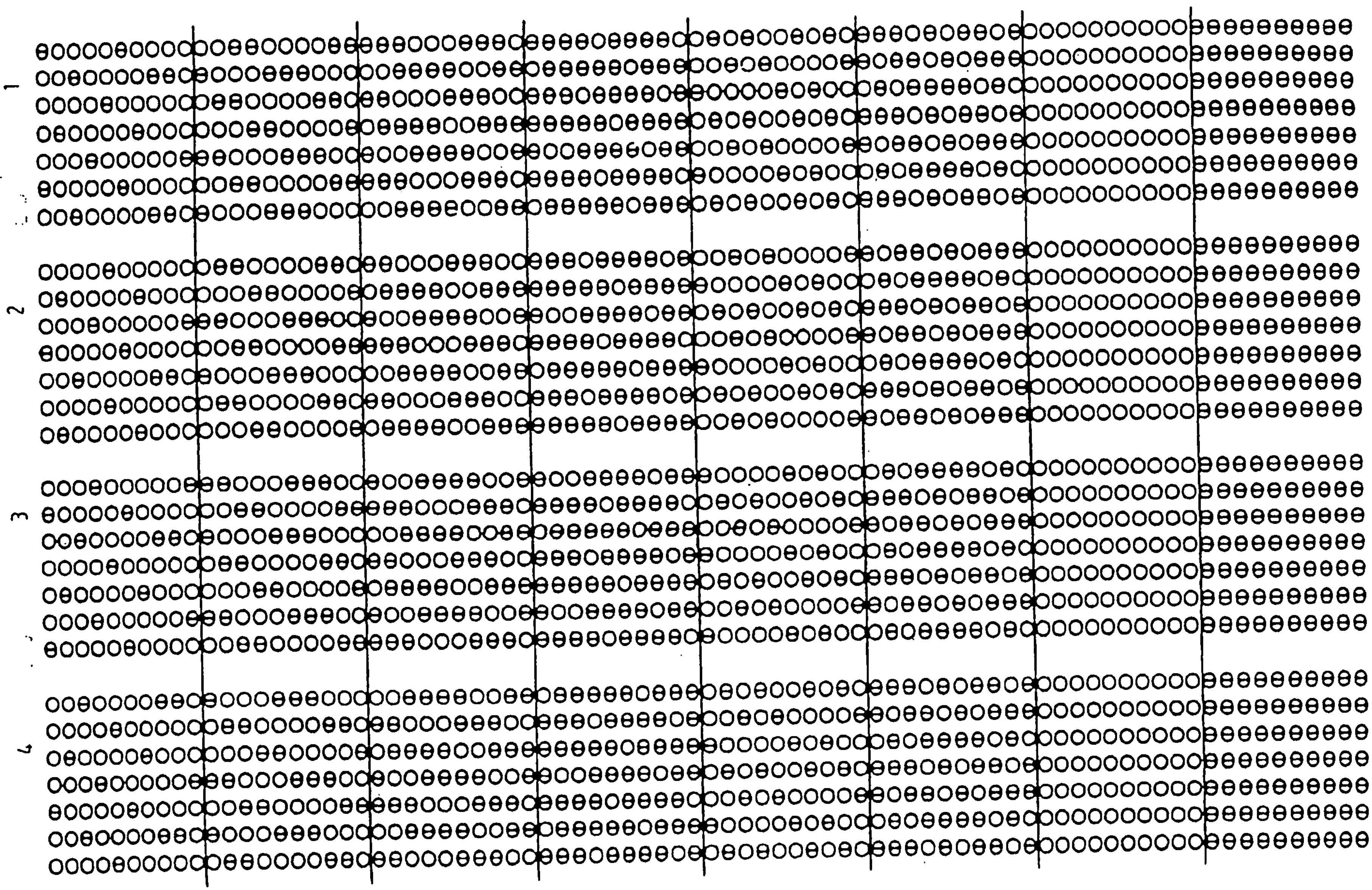


Fig. 14

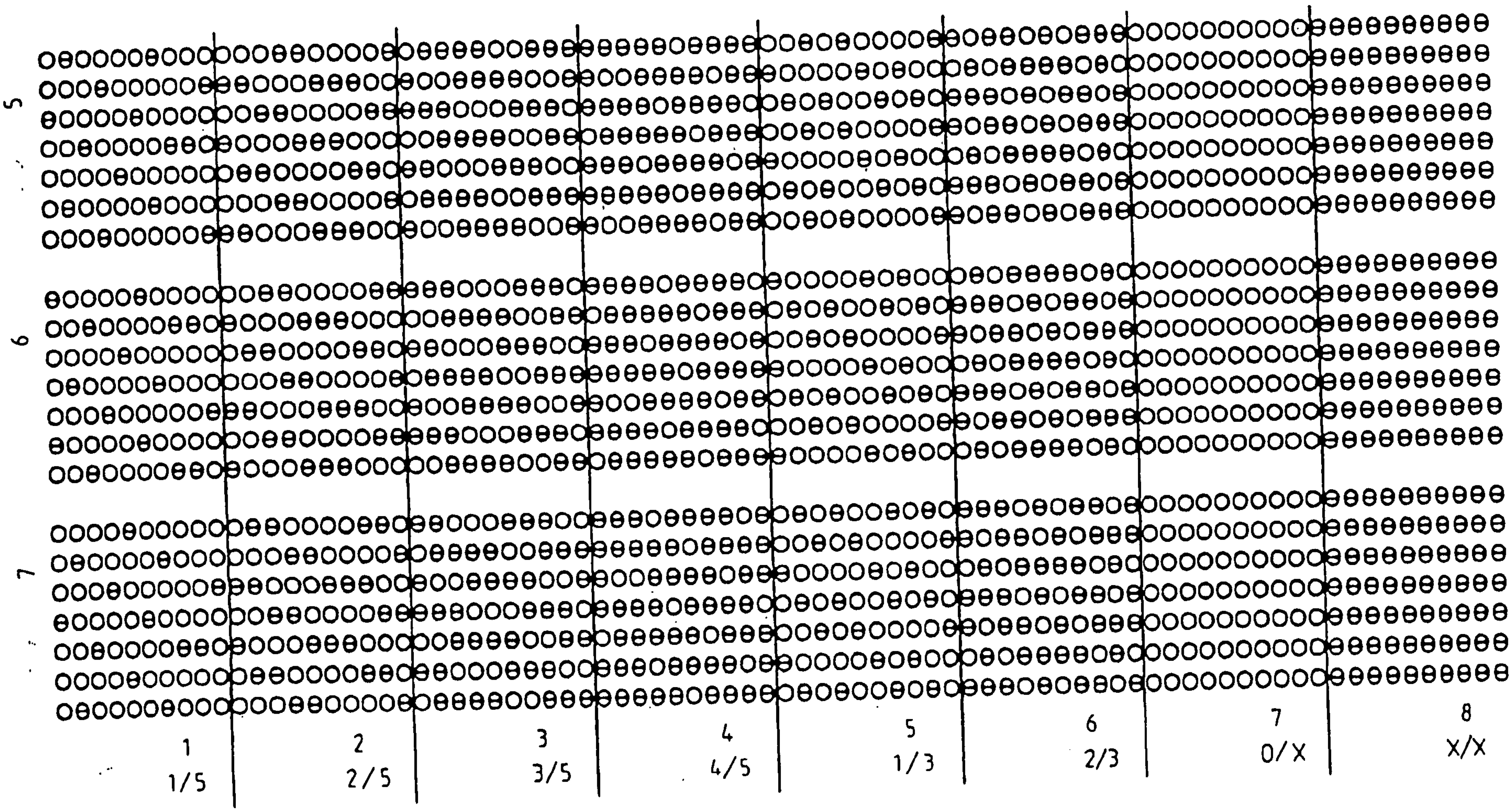


Fig.14A